# CLAIMS

1. A semiconductor structure formed on a surface of a substrate, comprising:

an active region formed in the substrate;

an epitaxial post formed on the surface of the substrate over the active region, the epitaxial post having at least one surface extending outwardly from the surface of the substrate and further having a surface opposite of the surface of the substrate;

a gate structure formed adjacent to at least a portion of all the outwardly extending surfaces of the epitaxial post; and

a capacitor formed on an exposed surface of the epitaxial post.

2. The semiconductor structure of claim 1, further comprising an insulating layer formed over portions of all the outwardly extending surfaces of the epitaxial post not covered by the gate structure.

3. The semiconductor structure of claim 1 wherein the gate structure comprises:

a gate oxide formed on all of the outwardly extending surfaces of the epitaxial post; and

a polysilicon gate formed on the gate oxide.

4. The semiconductor structure of claim 1, further comprising:

a insulating layer formed over the active region;

an opening through the insulating layer to expose a portion of the active region; and

a conductive material formed in the opening and on the active region to be electrically coupled thereto.

5. The semiconductor structure of claim 1, further comprising an insulating material formed over the gate structure to electrically insulate the gate structure.

6. The semiconductor structure of claim 1 wherein the active region comprises a buried digit line.

7. The semiconductor structure of claim 1 wherein the capacitor comprises a container shaped capacitor structure.

8. The semiconductor structure of claim 1 wherein the epitaxial post comprises an epitaxial post having a polygonal cross-sectional area.

9. A memory cell formed on a substrate having a surface, comprising:

an active region formed in the substrate;

a vertical transistor formed in an epitaxial post formed on the substrate surface and extending from the surface of the substrate, the vertical transistor further having a gate formed around a perimeter of the epitaxial post; and

a capacitor formed on the vertical transistor.

10. The memory cell of claim 9 wherein the vertical transistor comprises:

a gate oxide formed on a surface defining the perimeter of the epitaxial post;

gate formed on the gate oxide; and

insulating sidewalls formed on the gate.

11. The memory cell of claim 9 wherein the capacitor comprises a container shaped capacitor structure.

12. The memory cell of claim 9 wherein the memory cell of claim 201 further comprises a diffusion region in the epitaxial post adjacent the capacitor.

13. The memory cell of claim 9 wherein the active region comprises a buried digit line.

14. The memory cell of claim 9, further comprising a digit line contact formed over the active region and proximate the vertical transistor.

15. The memory cell of claim 9, further comprising an insulating region formed around the perimeter of the epitaxial post, and interposed between the capacitor and the vertical transistor.

16. A memory array formed on a surface of a substrate, comprising:

a plurality of active regions formed in the surface of the substrate;

a plurality of memory cell pairs formed in a respective active region, each of the memory cell pairs comprising first and second memory cells, each cell having a vertical transistor having a conductive channel with a first end proximate to the surface of the substrate and a second end opposite the first end, a capacitor formed on the vertical transistor proximate the second end of the channel, and a diffusion region interposed between the capacitor and the second end of the channel of the vertical transistor.

17. The memory array of claim 16 wherein the plurality of memory cell pairs further include a digit line contact formed on the respective active region.

18. The memory array of claim 16 wherein the capacitor comprises a container shaped capacitor structure.

19. The memory array of claim 16 wherein the vertical transistor comprises:

an epitaxial post formed on the active region and having at least one surface extending outwardly from the surface of the substrate, the diffusion region formed in the epitaxial post;

a gate oxide formed over a portion of all the outwardly extending surfaces of the epitaxial post; and

a polysilicon gate formed on the gate oxide.

20. The memory array of claim 16, further comprising buried digit lines coupling together the active regions associated with a column of memory.

21. A memory device having an address bus and a data terminal, comprising:

an array of memory cells formed on a substrate including silicon, the memory cells arranged in rows and columns, each of the rows having a word line and each of the columns having a bit line;

a row address circuit coupled to the address bus for activating the word line in the array corresponding to a row address applied to the row address circuit through the address bus;

a column address circuit coupled to the address bus for coupling an I/O line for the array to the bit line corresponding to a column address applied to the column address circuit through the address bus; and

a sense amplifier having an input coupled to a data line and an output coupled to the data terminal of the memory device, wherein each memory cell comprises:

an active region formed in the substrate;

an epitaxial post formed on the surface of the substrate over the active region, the epitaxial post having at least one surface extending outwardly from the surface of the substrate and further having a surface opposite of the surface of the substrate;

a transfer gate formed adjacent to at least a portion of all the outwardly extending surfaces of the epitaxial post; and

a memory cell capacitor formed on an exposed surface of the epitaxial post.

22. The memory device of claim 21 wherein the memory cells further comprise an insulating layer formed over portions of all the outwardly extending surfaces of the epitaxial post not covered by the transfer gate.

23. The memory device of claim 21 wherein the transfer gate of the memory cells comprises:

a gate oxide formed on all of the outwardly extending surfaces of the epitaxial post; and

a polysilicon gate formed on the gate oxide.

24. The memory device of claim 21 wherein the of the memory cells further comprise:

a insulating layer formed over the active region;

an opening through the insulating layer to expose a portion of the active region; and

a conductive material formed in the opening and on the active region to be electrically coupled thereto.

25. The memory device of claim 21 wherein the of the memory cells further comprise an insulating material formed over the transfer gate to electrically insulate the transfer gate.

26. The memory device of claim 21 wherein the active region of the memory cells comprises a buried digit line.

27. The memory device of claim 21 wherein the memory cell capacitor of the memory cells comprises a container shaped capacitor structure.

28. The memory device of claim 21 wherein the epitaxial post of the memory cells comprises an epitaxial post having a polygonal cross-sectional area.

29. A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus and adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus and adapted to allow data to be output from the computer system; and

a memory device coupled to the processor through the processor bus, the memory device comprising:

an array of memory cells formed on a substrate including silicon, the memory cells arranged in rows and columns, each of the rows having a word line and each of the columns having a bit line;

a row address circuit coupled to the address bus for activating the word line in the array corresponding to a row address applied to the row address circuit through the address bus;

a column address circuit coupled to the address bus for coupling an I/O line for the array to the bit line corresponding to a column address applied to the column address circuit through the address bus; and

a sense amplifier having an input coupled to a data line and an output coupled to the data terminal of the memory device, wherein each memory cell comprises:

an active region formed in the substrate;

an epitaxial post formed on the surface of the substrate over the active region, the epitaxial post having at least one surface extending outwardly from the surface of the substrate and further having a surface opposite of the surface of the substrate;

a transfer gate formed adjacent to at least a portion of all the outwardly extending surfaces of the epitaxial post; and

a memory cell capacitor formed on an exposed surface of the epitaxial post.

30. The computer system of claim 29 wherein the memory cells of the memory device further comprise an insulating layer formed over portions of all the outwardly extending surfaces of the epitaxial post not covered by the transfer gate.

31. The computer system of claim 29 wherein the transfer gate of the memory device comprises:

a gate oxide formed on all of the outwardly extending surfaces of the epitaxial post; and

a polysilicon gate formed on the gate oxide.

32. The computer system of claim 29 wherein the memory cells of the memory device further comprise:

a insulating layer formed over the active region;

an opening through the insulating layer to expose a portion of the active region; and

a conductive material formed in the opening and on the active region to be electrically coupled thereto.

33. The computer system of claim 29 wherein the memory cells of the memory device further comprise an insulating material formed over the transfer gate to electrically insulate the transfer gate.

34. The computer system of claim 29 wherein the active region of the memory device comprises a buried digit line.

35. The computer system of claim 29 wherein the memory cell capacitor of the memory device comprises a container shaped capacitor structure.

36. The computer system of claim 29 wherein the epitaxial post of the memory device comprises an epitaxial post having a polygonal cross-sectional area.

37. A method for forming a semiconductor structure on a surface of a substrate, comprising:

forming an active region in the substrate;

forming an epitaxial post on the substrate over the active region, the epitaxial post having at least one surface extending outwardly from the surface of the substrate and further having a surface opposite of the surface of the substrate;

forming a gate structure adjacent to at least a portion of all the outwardly extending surface of the epitaxial post; and

forming a capacitor on the exposed surface of the epitaxial post.

38. The method of claim 37 wherein forming the epitaxial post comprises:

forming first and second sacrificial structures spaced laterally apart on the substrate;

forming sidewalls on the first and second sacrificial structures to define a trench region therebetween, the surface of the substrate exposed in the trench region;

forming an epitaxial layer on the exposed surface of the substrate in the trench region.

39. The method of claim 38 wherein forming the gate structure comprises:

removing the sidewalls on the first and second sacrificial structures to define a gap between the sacrificial structures and the epitaxial post;

forming a gate oxide over exposed surfaces of the epitaxial post;

depositing polycrystalline silicon in the gap region;

recessing the polycrystalline silicon below an upper surface of the epitaxial post; and

forming an insulating region on the polycrystalline silicon in the gap between the polycrystalline silicon and the upper surface of the epitaxial post.

40. The method of claim 37 wherein forming the capacitor comprises:

forming a first layer of doped polycrystalline silicon on the surface opposite of the surface of the surface of the substrate of the epitaxial post;

diffusing dopants from the first layer of doped polycrystalline silicon to the epitaxial post;

forming a capacitor dielectric layer over the first layer of doped polycrystalline silicon; and

forming a second layer of doped polycrystalline silicon on the capacitor dielectric layer.

41. The method of claim 37, further comprising:

depositing an insulating interlayer over the gate structure;

opening a via through the insulating interlayer to expose a portion of the active region; and

depositing a conductive material over the insulating interlayer and into the opening to contact the exposed portion of the active region.

42. The method of claim 37 wherein forming the active region comprises forming buried digit lines in the substrate.

43. A method for forming pair of memory cells on a surface of the substrate, comprising:

forming an active region in the substrate;

forming a vertical transistor in an epitaxial post formed on the substrate surface and extending from the surface of the substrate, the vertical transistor further having a gate formed around a perimeter of the epitaxial post; and

forming a capacitor on the vertical transistor.

44. The method of claim 43 wherein forming the vertical transistor comprises:

forming a gate oxide on a surface defining the perimeter of the epitaxial post;

forming a gate on the gate oxide; and

forming insulating sidewalls on the gate.

45. The method of claim 43 wherein the forming the capacitor comprises forming a container shaped capacitor structure.

46. The method of claim 43, further comprising forming a diffusion region in the epitaxial post adjacent the capacitor.

47. The method of claim 43 wherein forming the active region comprises forming a buried digit line.

48. The method of claim 43, further comprising forming a digit line contact over the active region and proximate the vertical transistor.

49. The method of claim 43, further comprising forming an insulating region around the perimeter of the epitaxial post, and interposed between the capacitor and the vertical transistor.